A Modular Single-Phase Power-Factor-Correction Scheme With a Harmonic Filtering Function

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***Abstract*—Power supply systems in telecommunication applications employ several parallel-connected ac-to-dc and dc-to-dc power converters. Such a system offers modularity, redundancy, and is easily scalable to higher power levels. Such parallel-connected systems normally consist of several single-phase power-factor-correction (PFC) stages connected to the same input utility. In this paper, a modular single-phase PFC scheme with an integrated harmonic filtering function is presented. The proposed approach demonstrates that, with suitable modifications to the PFC control, harmonic filtering capability can be added. In other words, the PFC stage can compensate for harmonics generated by other rectifier loads connected to the same ac input terminals. The paper presents an example employing three ac–dc rectifier stages with only one ac–dc rectifier stage with PFC capability. It is shown that one PFC stage with the proposed control can compensate for harmonics generated by the other two uncompensated rectifier stages. Results from a laboratory prototype system demonstrate that the overall system meets the EN 61000-3-2 harmonic limits.**

***Index Terms*—Digital signal processor (DSP), harmonic filtering, modular, nonlinear load, power-factor correction (PFC).**

I. Introduction

THE recent developments in power electronics technology enable us to introduce power converters into telecommunication applications to drive various loads in single-phase power distribution systems. The expanding use of electric loads controlled by power electronics has made power converters an important and unquestionable part of the modern society. Power supply systems in telecommunication applications employ several parallel-connected ac-to-dc and dc-to-dc power converters. Such a system offers modularity, redundancy, and is easily scalable to higher power levels. Such parallel-connected systems normally consist of several single-phase power-factor-correction (PFC) stages connected to the same input utility as shown in Fig. 1 [1]–[3]. Therefore, the system cannot accomplish low-cost power supply and its control could be complicated. In order to solve the problem, the diode rectifier is the most utilized in industrial and commercial applications for economic reasons even though this rectifier employed in power electronic equipment has a poor power factor and generates much harmonics owing to having an electrolytic capacitor in its dc link. Great effects are paid for making its input current waveform sinusoidal, otherwise it may give rise to serious problems in the power systems [4]. To comply with the corresponding standards in Europe and America, several active solutions have been proposed [5] and widely studied in the literature. These standards are most usually employed in the design of a boost converter (BC). The design of the power converters requires many features such as the following:

1) small input current harmonics to minimize losses;
2) high input power factor to minimize reactive requirements;
3) minimum conducted electromagnetic interference (EMI).

Power-factor-corrected switch-mode-type preregulators are desirable since they provide good features such as a high power factor, a low harmonic content in input current, a fast dynamic response, and low cost.

In this paper, a modular single-phase PFC scheme with an integrated harmonic filtering function is presented. By employing only one PFC stage and other nonlinear loads (NLs) such as a diode rectifier, the PFC stage fulfills PFC and harmonic current compensation. Therefore, the PFC circuit can be used to eliminate unwanted harmonic currents by injecting additional currents and improve the input power factor of the telecommunication rectifier system. The advantages of the proposed approach are as follows.

- Only one PFC stage is employed to compensate for harmonics generated by other diode rectifier loads connected to the same utility.
- The PFC stage fulfills PFC and harmonic current compensation.
- Control of PFC can be simplified.

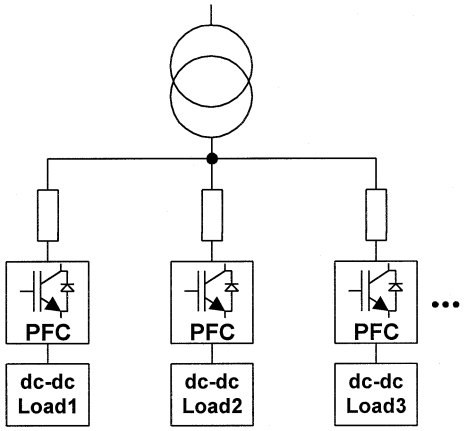

Fig. 1. Typical multiconverter system for Telecom rectifier.

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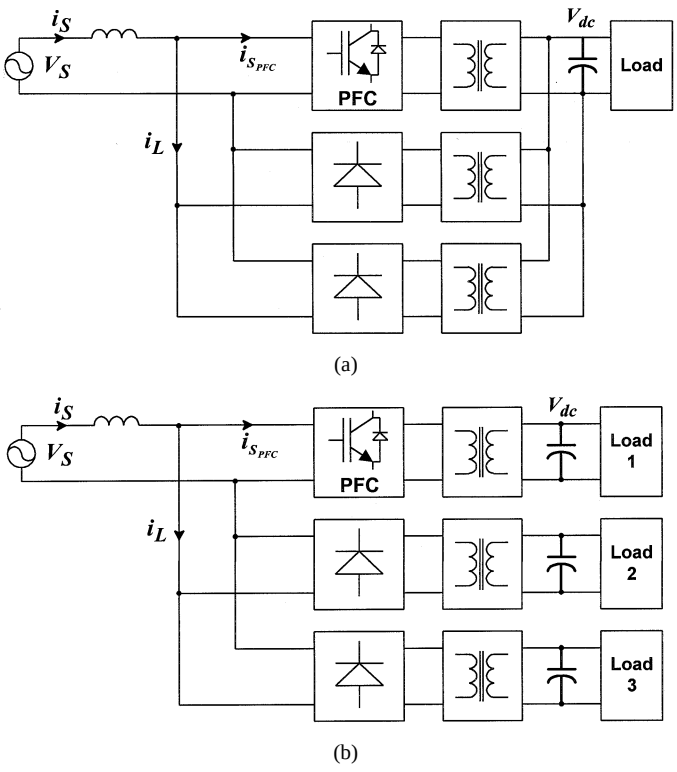

Fig. 2. Modular single-phase PFC scheme. (a) Module with shared dc link. (b) Module with independent dc link.

- The proposed modular scheme is compact and its cost is low.
- This scheme is applicable to telecommunication rectifier systems.

To achieve fast real-time processing of the control algorithm, a fixed-point TI DSP-TMS320LF2407, is used for implementation. Results from a laboratory prototype system demonstrate that the overall system meets the EN 61000-3-2 harmonic limits.

II. Proposed Topology

The typical converter system in telecommunication applications has several PFC circuits in parallel as shown in Fig. 1. Such a system can be replaced by either dc-link shared or independent modular scheme which consists of several ac-to-dc and dc-to-dc power converters employing only one PFC circuit and several NLs. Fig. 2 shows the possible combination with isolated converter. Each scheme is capable of achieving unity power factor with sinusoidal current waveform by injecting harmonic current through a PFC circuit [6], [7]. Fig. 3 shows the proposed telecommunication PFC-BC paralleled with nonlinear loads and its waveforms. The input source current is defined as

$$i_s = i_{s_{\mathrm{PFC}}} + i_L \tag{1}$$

where i_s, i_L, and $i_{s_{\mathrm{PFC}}}$ are a source, nonlinear load, and PFC boost converter current, respectively. Typically, the current spectrum of nonlinear loads has a fundamental component, third, fifth, seventh, and so on. Therefore, the PFC current should contain the same harmonics as the NLs and also supply its own power. It has a fundamental component which is shown in Section III.

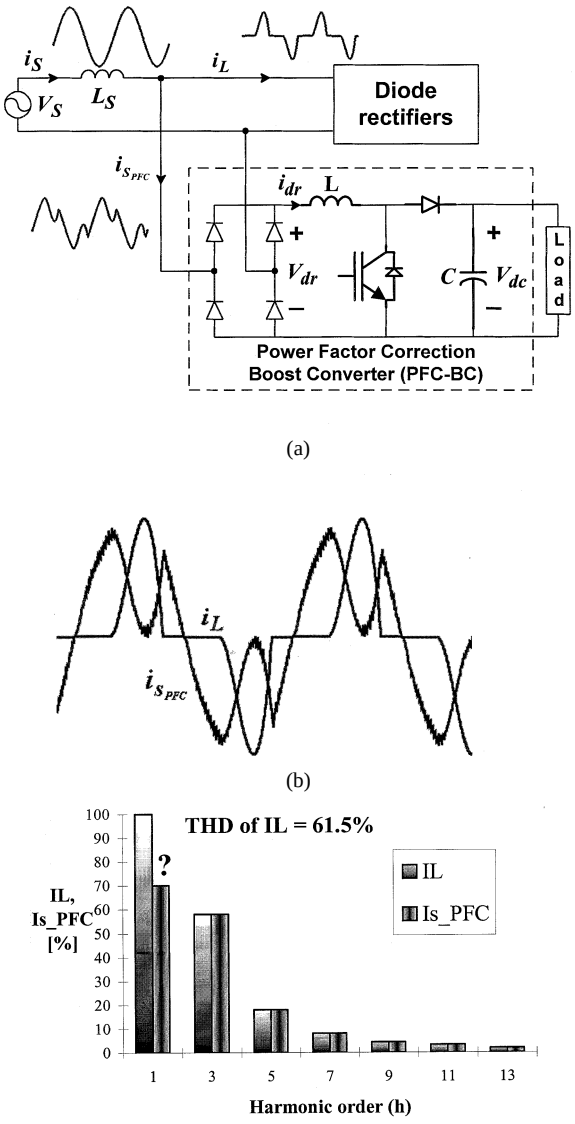

Fig. 3. Proposed PFC-BC with harmonic current compensation. (a) Topology. (b) Waveforms. (c) Spectrum of typical diode rectifier and PFC current.

III. Principle of Operation and Analysis

Since the fundamental current shown in Fig. 4(a) is expressed with a displacement power-factor angle ϕ, the PFC current must contain a leading power angle ψ to compensate for the reactive power of the NLs

$$i_{L1} = \sqrt{2} I_{L1} \sin(\omega t - \phi), \tag{2}$$

$$i_{s_{\mathrm{PFC}}1} = \sqrt{2} I_{s_{\mathrm{PFC}}1} \sin(\omega t + \psi) \tag{3}$$

where I_{L1} and $I_{s_{\mathrm{PFC}}1}$ are the fundamental rms values of NLs and PFC converter, respectively. The PFC fundamental current $I_{s_{\mathrm{PFC}}1}$ is determined by the PFC load and the displacement power-factor angle ϕ between V_s and I_{L1}. The harmonic components are given by

$$i_{Lh} = \sum_{n=3,5,7\ldots} \sqrt{2} I_{Ln} \cdot \sin(n\omega t + \phi_n) \tag{4}$$

$$i_{s_{\mathrm{PFC}}h} = -\, i_{Lh} \tag{5}$$

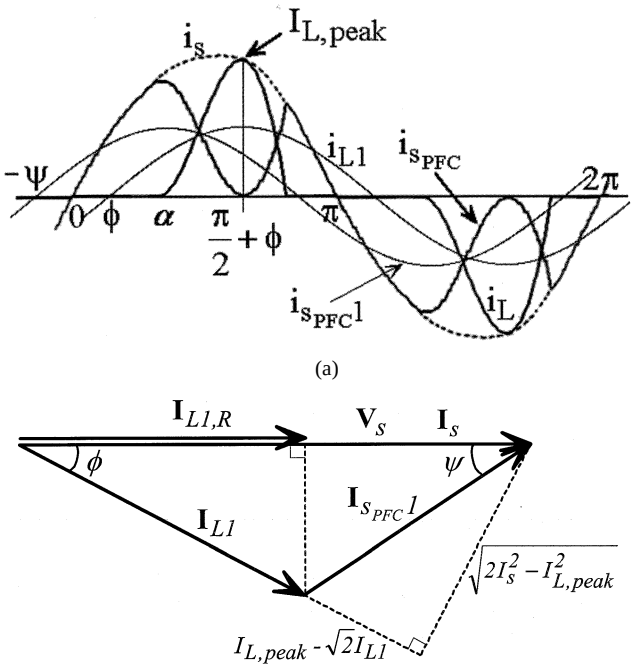

Fig. 4. Analysis of harmonic currents. (a) Waveforms. (b) Current vectors.

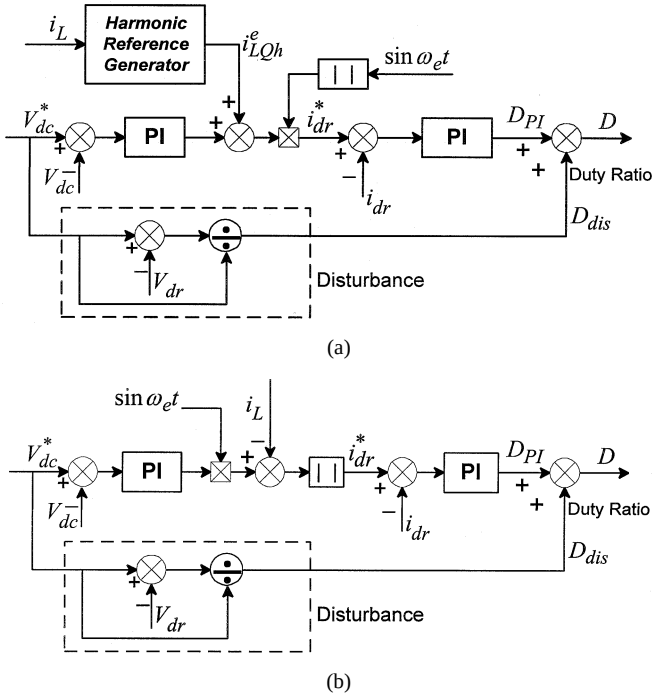

Fig. 5. Control block diagram for the proposed PFC-BC. (a) With harmonic reference generator. (b) Without harmonic reference generator.

where the subscript h denotes the harmonic current. Thus, the harmonic components $i_{s_{\rm PFC}h}$ of the PFC equal those of the NLs to make the utility current sinusoidal. Therefore, PFC current $i_{s_{\rm PFC}}$ contains the fundamental and also the harmonics of the NLs

$$I_{s_{\rm PFC}} = \sqrt{I^2_{s_{\rm PFC}1} + I^2_{Lh}} \tag{6}$$

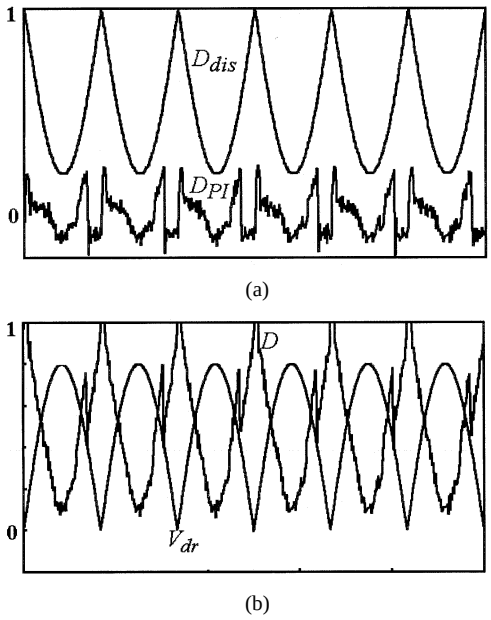

Fig. 6. Waveforms of control system parameters. (a) D_{dis} and $D_{\rm PI}$. (b) Duty ratio D and rectified voltage V_{dr}.

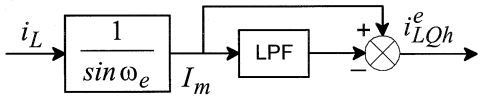

Fig. 7. Block diagram for harmonic reference current generator.

where the rms current for harmonics is defined as

$$I_{Lh} = \sqrt{\sum_{n=3,5,7...} I^2_{Ln}}. \tag{7}$$

Assuming the angle at the point where the nonlinear load current has a peak is $\pi/2+\phi$ or $3\pi/2+\phi$, and $\pi/2+\phi = \pi - \alpha$, and from the current vectors concerning fundamental components shown in Fig. 4(b), the minimum limit of the utility current I_s can be expected to be

$$I_s \geq \frac{I_{L,\rm peak}}{\sqrt{2}\cos\phi} \tag{8}$$

where I_s is the rms current on the utility side. The crest factor of i_L can be defined as a ratio of the peak value to the total rms current

$$CF = \frac{I_{L,\rm peak}}{I_{L,\rm rms}}. \tag{9}$$

From the definition of total harmonic distortion (THD) of i_L, $I_{L,\rm peak}$ is derived as

$$I_{L,\rm peak} = I_{L1} \cdot CF \cdot \sqrt{1 + \rm THD^2_{NL}} \tag{10}$$

where $\rm THD_{NL}$ is the THD of the NLs. The current vectors can be written as

$$\begin{aligned} \mathbf{I}_s &= \sqrt{2} I_s \angle 0^\circ \\ \mathbf{I}_{L1} &= \sqrt{2} I_{L1} \angle \phi \\ \mathbf{I}_{s_{\rm PFC}1} &= \sqrt{2} I_{s_{\rm PFC}1} \angle -\psi \end{aligned} \tag{11}$$

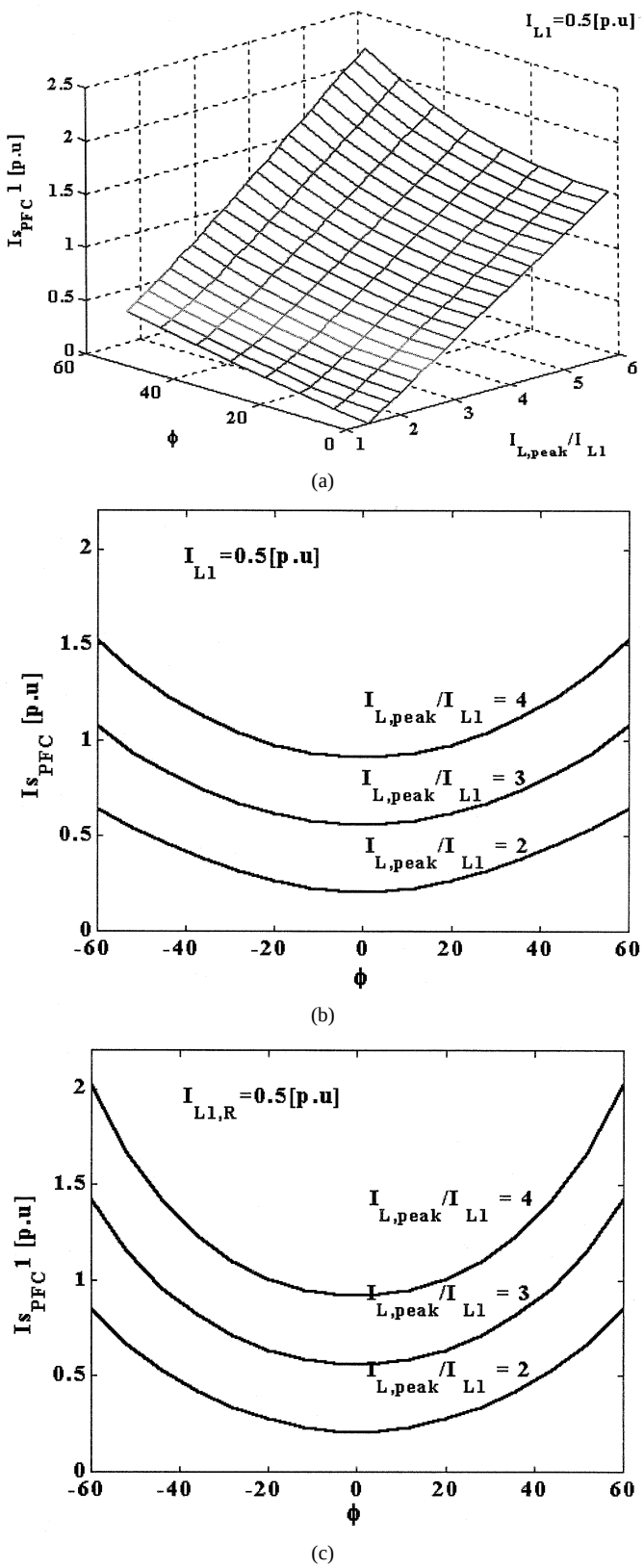

Fig. 8. Fundamental component calculation of Boost converter. (a) Minimum required fundamental current of $i_{s_{\rm PFC}}$. (b) With constant input power. (c) With constant NL.

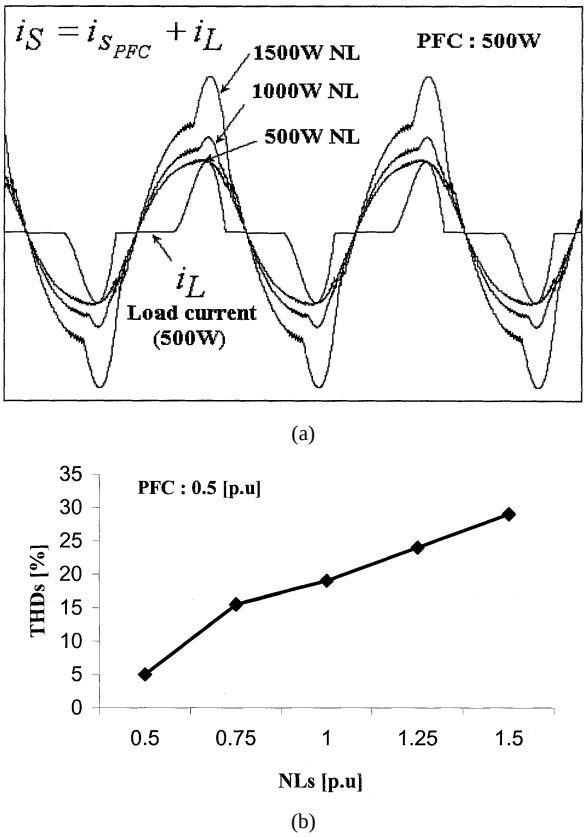

Fig. 9. Utility current waveforms in terms of nonlinear load change. (a) Current waveforms. (b) Total harmonic distortion.

TABLE I
EN 61000-3-2 HARMONIC CURRENT LIMITS WITH $I_1 \leq 16$ A

n	*230 (V)* I_n (A)	*120 (V)* I_n (A)
3	2.30	4.42
5	1.14	2.19
7	0.77	1.48
9	0.40	0.77
11	0.33	0.63
13	0.21	0.40
15-39	2.25/n	4.35/n

where

$$\psi = \sin^{-1}\left(\frac{I_{L1}\sin\phi}{I_{s_{\rm PFC}1}}\right). \tag{12}$$

Therefore, from the current vectors, the minimum PFC fundamental current is obtained by

$$I_{S_{\rm PFC}1,\min} = \sqrt{I_s^2 - \sqrt{2}I_{L1}I_{L,\rm peak} + I_{L1}^2}. \tag{13}$$

By substituting (10) into (13), we arrive at (14), as shown at the bottom of the next page. Assuming that the nonlinear load power is constant, I_{L1} is expressed by employing its active component as

$$I_{L1} = \frac{I_{L1,R}}{\cos\phi}. \tag{15}$$

Therefore, (13) is replaced for the constant nonlinear loads

$$I_{S_{\rm PFC}1,\min} = \sqrt{\frac{1}{2}\left(\frac{I_{L,\rm peak}}{\cos\phi}\right)^2 - \sqrt{2}\frac{I_{L1,R}I_{L,\rm peak}}{\cos\phi} + \left(\frac{I_{L1,R}}{\cos\phi}\right)^2}. \tag{16}$$

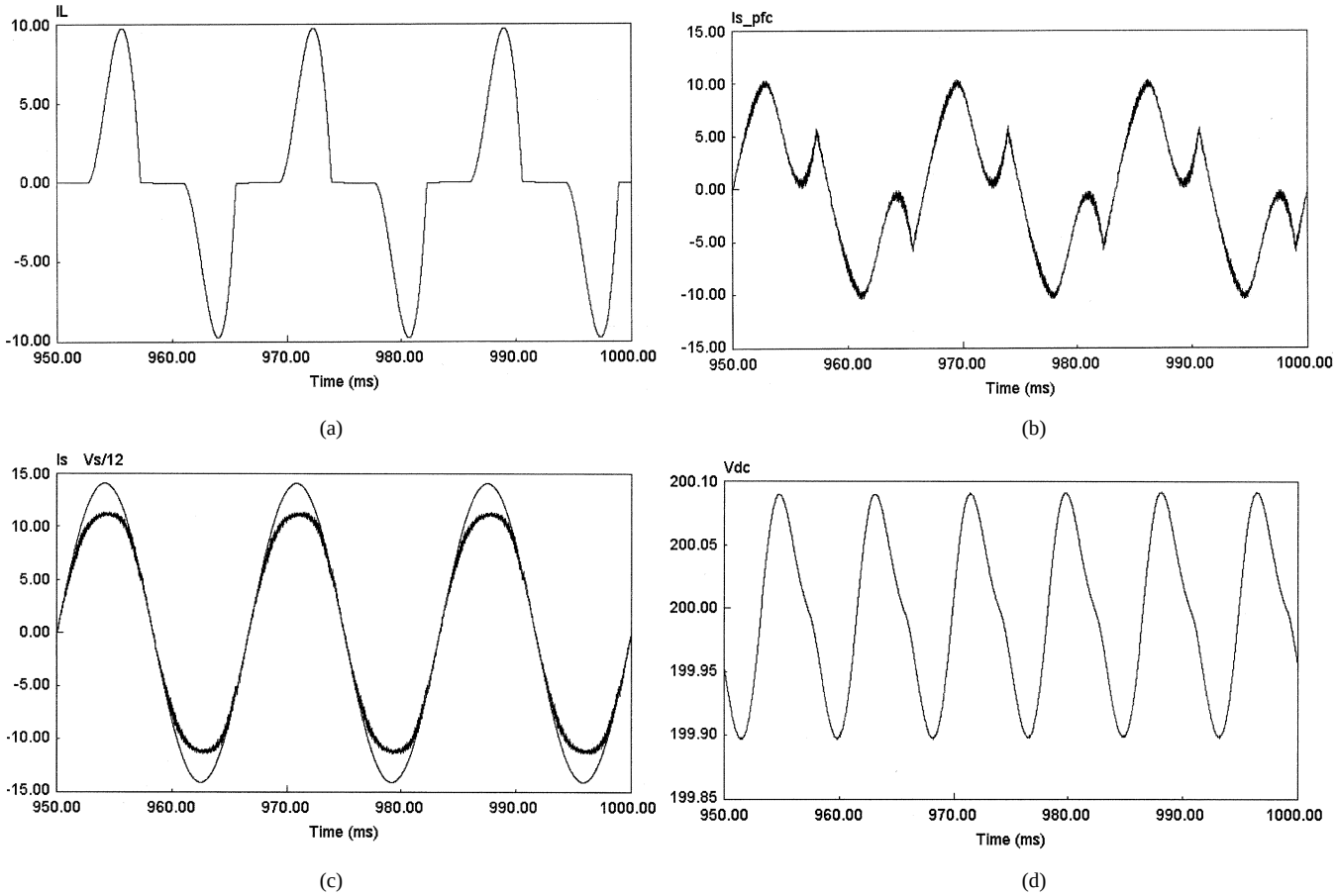

Fig. 10. Simulation results (PFC: 500 W; NL: 500 W). (a) Nonlinear load current. (b) PFC-BC current. (c) Utility current and voltage. (d) Output voltage of boost converter.

If the boost converter load is suddenly reduced or the nonlinear loads are increased, the system cannot compensate for all the harmonic components. In this case, the PFC current $i_{s_{\rm PFC}}$ must satisfy the condition as

$$V_s i_{s_{\rm PFC}} \geq 0 \tag{17}$$

otherwise, $i_{s_{\rm PFC}} = 0$.

IV. Controller Design

The control block diagram for the PFC boost converter is shown in Fig. 5 with and without current reference generator. Fig. 5(a) introduces the principle for the harmonic compensation and Fig. 5(b) shows a simple control block diagram which can be easily implemented by analog circuits. The control block diagram consists of a dc-voltage proportional-plus-integral (PI) controller, current controller, harmonic reference current generator, and the disturbance. The rectified voltage V_{dr} can be considered as a disturbance since the input voltage of the boost converter is basically a dc quantity. Based on the rectified voltage and constant reference dc-link voltage, a duty ratio is obtained as

$$D_{dis} = \frac{V_{\rm dc}^* - V_{dr}}{V_{\rm dc}^*} \tag{18}$$

where D_{dis} is the open-loop duty ratio and $V_{\rm dc}^*$ is the reference dc-link voltage. The closed-loop duty ratio $D_{\rm PI}$, which contains a small amount of variations depending on load conditions, is obtained from current control. The switch gate input, or final duty ratio D, is derived as

$$D = D_{\rm PI} + D_{dis}. \tag{19}$$

The parameters are shown in Fig. 6. Since $D_{\rm PI}$ takes care of current regulation with low variations, the bandwidth of the control loop can be increased. A block diagram for the harmonic reference current generator is shown in Fig. 7 [6]. In order to subtract the fundamental component from the current of rectifier loads, the low-pass filter is designed on the synchronous reference frame with the fundamental angular frequency of the

$$I_{S_{\rm PFC}1,\min} = I_{L1}\sqrt{\frac{CF^2(1+{\rm THD}_{NL}^2)}{\cos^2\phi} - \frac{\sqrt{2}CF\sqrt{1+{\rm THD}_{NL}^2}}{\cos\phi} + 1} \tag{14}$$

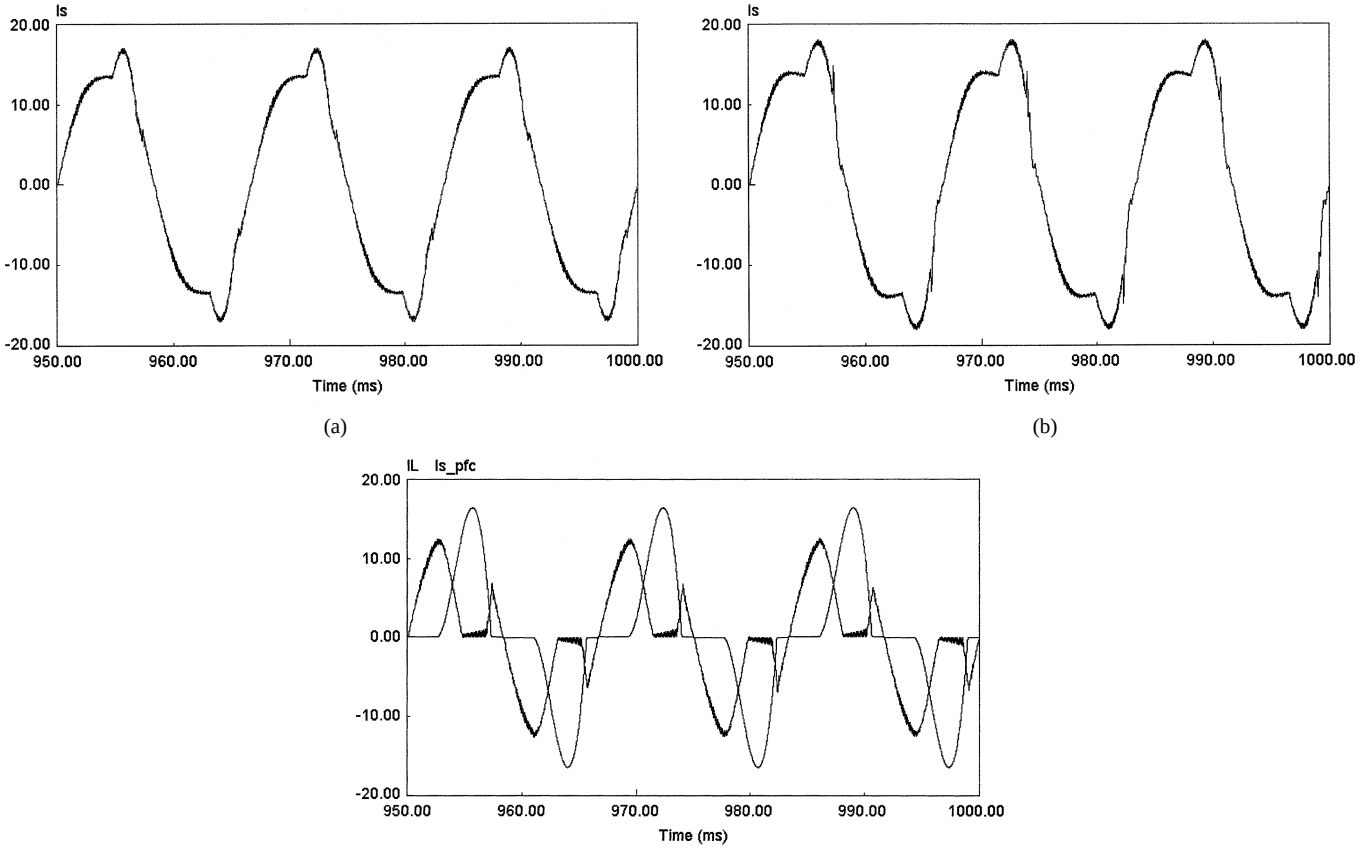

Fig. 11. Simulation results (PFC: 500 W). (a) Utility current (NL: 700 W; total: 1.2 kW). (b) Utility current (NL: 1000 W; total: 1.5 kW). (c) NL and PFC-BC currents (700 W NL).

utility, ω_e. A reference harmonic current for the boost converter is obtained by

$$i_{dr}^{*} = |\kappa \sin \omega t - i_L| \tag{20}$$

where κ is given from the PI voltage controller.

V. Design Example

The proposed PFC rectifier circuit is designed according to the following parameters:

$$\begin{aligned}
\text{total output power } (P_o) &= 1000 \text{ W} = 1 \text{ p.u.} \\
\text{input voltage } (V_s) &= 120 \text{ V} = 1 \text{ p.u.} \\
\text{input current } (I_s) &= \frac{1000}{120} = 8.3 \text{ A} = 1 \text{ [p.u} \\
\text{base impedance } (Z_b) &= 14.5\ \Omega = 1 \text{ p.u.} \\
\text{line frequency} &= 60 \text{ Hz.}
\end{aligned}$$

Boost PFC:

$$\begin{aligned}
\text{output power rating} &= 500 \text{ W} = 0.5 \text{ p.u} \\
\text{boost inductance } (L_{dr}) &= 1.4 \text{ mH} = 0.036 \text{ p.u.} \\
\text{dc capacitance } (C_{\text{dc}}) &= 1 \text{ mF} = 5.5 \text{ p.u.} \\
\text{switching frequency} &= 32.768 \text{ kHz} \\
\text{dc output voltage } (V_{\text{dc}}) &= 240 \text{ Vdc} = 2 \text{ p.u.}
\end{aligned}$$

Diode rectifier:

$$\begin{aligned}
\text{output power rating} &= 500 \text{ W} = 0.5 \text{ p.u.} \\
\text{dc inductance } (L_d) &= 2.8 \text{ mH} = 0.073 \text{ p.u} \\
\text{dc capacitance } (C_{\text{dc}}) &= 3.3 \text{ mH} = 18 \text{ p.u.}
\end{aligned}$$

Fig. 8 shows that the fundamental component of the PFC boost converter which is designed based on the displacement power-factor angle ϕ and the peak value of NLs is calculated from (13) and (16). Assuming that $\cos\phi = 0.95$, $I_{L1,R} = 0.5$ p.u, $\text{THD}_{\text{NL}} = 0.6$, the total current ratings of PFC boost converter and NLs can be calculated from (6)

$$\begin{aligned}
I_{s_{\text{PFC}}} &= \sqrt{I_{s_{\text{PFC}}1}^2 + \text{THD}_{NL}^2 \frac{I_{L1,R}^2}{\cos^2\phi}} \\
&= \sqrt{0.5^2 + 0.6^2 \frac{0.5^2}{0.95^2}} \\
&= 0.59 \text{ p.u.} \\
I_L &= \frac{0.5}{0.95}\sqrt{1 + 0.6^2} \\
&= 0.61 \text{ p.u.}
\end{aligned}$$

Once the proposed converter is designed with 0.5-p.u. PFC, it cannot compensate for all the harmonics of the NLs which are greater than 0.5 p.u. Fig. 9 shows the utility current waveforms and THDs as an example corresponding to different NLs. However, to meet the EN 61000-3-2 standard [8] which deals with low voltage and devices absorbing current of less than 16 A as

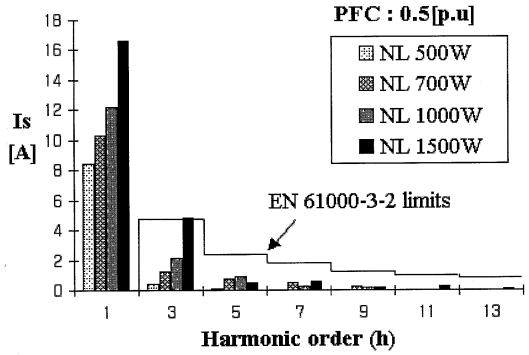

Fig. 12. Harmonic analysis of I_s from simulation results.

TABLE II
SIMULATION RESULTS

n	I_S (PFC:500W)			
	NL 0.5kW	NL 0.7kW	NL 1kW	NL 1.5kW
1	8.4	10.32	12.2	16.6
3	0.42	1.25	2.12	4.8
5	0.056	0.7	0.92	0.49
7	0.02	0.46	0.24	0.56
9	0.03	0.22	0.2	0.2
11	0.02	0.01	0.02	0.26
13	0.01	0.01	0.01	0.11
$I_{L,peak}/I_{L1}$	2.1	2.0	1.94	1.8
RMS	8.42	10.4	12.45	17.3
THD(%)	5.1	15	19	29.37

shown in Table I, the 1.5-p.u. converter can be designed with 0.5 p.u. of PFC and 1 p.u. of NLs.

VI. Simulation and Experimental Results

Simulation results are shown in Figs. 10 and 11. The PFC boost converter compensates for harmonics and reactive power given by nonlinear load and supplies the power to its own load. Fig. 12 shows that the input current of the proposed rectifier system can meet the EN 61000-3-2 harmonic limits as the NLs increase up to 1.2 p.u. with the 0.5 p.u. of PFC circuit. All the simulation results including input harmonic components, $I_{L,\text{peak}}/I_{LI}$, and THD are summarized in Table II. The control system is implemented by using digital signal processor (DSP) TMS320LF2407,[1] which has a function of fixed-point arithmetic. Also, analog control can be achieved due to a simple control block as shown in Fig. 5(b). Fig. 13 shows the experimental results from a laboratory prototype with different nonlinear loads.

VII. Conclusions

A modular single-phase PFC with a harmonic filtering function has been presented. It has been shown that a single-phase PFC scheme can be suitably altered to achieve harmonic filtering function of nonlinear loads connected to the system. The overall system to meet EN 61000-3-2 harmonic limits with the proposed approach should result in lower cost. Experimental results from a laboratory prototype system validate the PFC capability.

[1]TMS320F/C24X DSP Controller, Texas Instruments, Dallas, TX, 1999.

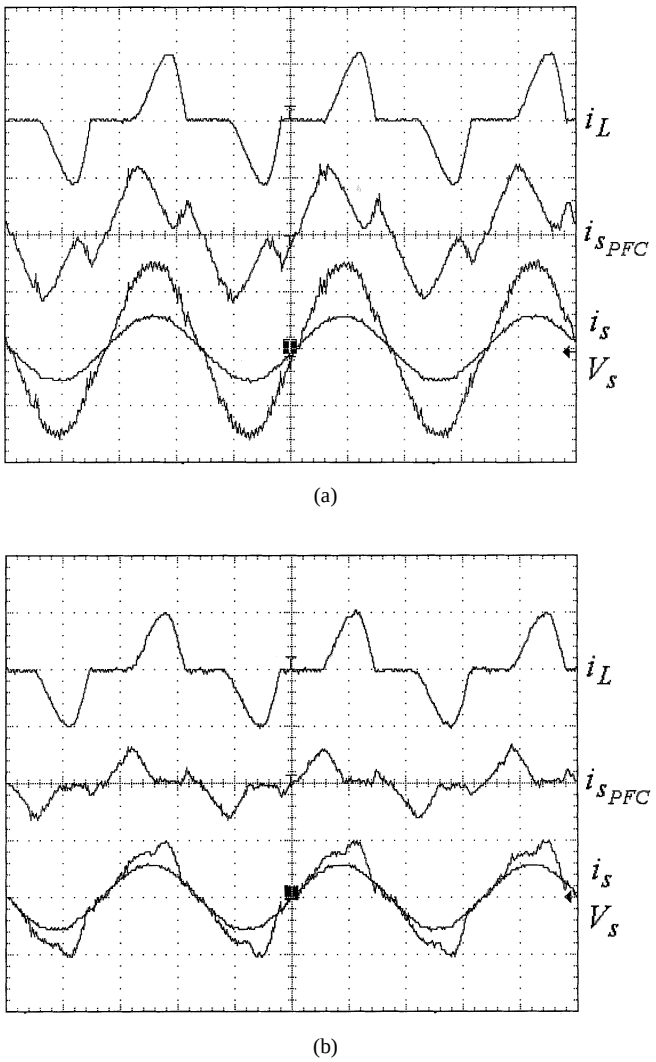

Fig. 13. Experimental results. (a) NLs: 0.5 p.u.; current: 5 A/div. (b) NLs: 0.7 p.u.; current: 10 A/div.

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Dr. Enjeti was the recipient of Second Best Paper Awards in 1993, 1998, 1999, and 2001, and a Third Best Paper Award in 1996 from the IEEE Industry Applications Society (IAS). He received the Second Prize Paper Award from the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS for papers published from mid-year 1994 to mid-year 1995 and the *IEEE Industry Applications Magazine* Prize Article Award in the year 1996. He is a Member of the IAS Executive Board and the Chair of the Standing Committee on "Electronic Communications." He was also the recipient of the select title "Class of 2001 Texas A&M University Faculty Fellow" for demonstrated achievement of excellence in research, scholarship, and leadership in the field. He directed a team of students to design and build a low-cost fuel cell inverter for residential applications, which won the 2001 Future Energy Challenge Award, Grand Prize, from the U.S. Department of Energy. He is a Registered Professional Engineer in the State of Texas.