Active Harmonic Rectifier (AHR) to Improve Utility Input Current THD in Telecommunication Power Distribution System

Abstract

The modern telecommunication power supply systems have several parallel-connected switch-mode rectifiers to provide 48Vdc. A typical switch-mode rectifier configuration includes a three-phase diode rectifier followed by a dc–dc converter. Such a system draws significant harmonic currents for the utility, resulting in poor input power factor and high total harmonic distortion. In this project, a three-phase active harmonic rectifier (AHR) scheme is proposed. In the AHR scheme, a diode rectifier module is replaced by a six-insulated-gate-bipolar-transistor/MOSFET based pulse width-modulation rectifier to supply load harmonics as well as its own active power. Each dc–dc converter module is connected to a shared 48-V dc link. The AHR module together with parallel-connected switch-mode rectifiers is controlled to achieve clean input power characteristics. The VA ratings of the AHR scheme is compared with an active power filter approach. The control design is based on linear control technique approach. Analysis, simulation, and experimental results show that the AHR offers several advantages such as lower VA rating, better current control response, efficient use of the AHR dc link, small size, and stable dc-link voltage control.
Chapter 1

1. Introduction

Modern telecommunication power systems require several three-phase rectifiers in parallel to obtain higher dc power with 48 Vdc. Such a rectifier normally employs diodes or silicon-controlled rectifiers (SCR) to interface with the electric utility due to economic reasons. The rectifier-type utility interface causes significant harmonic currents, resulting in poor input power factor and high total harmonic distortion (THD), which contributes to an inefficient use of electric energy. The above-mentioned rectifier is referred to as a nonlinear load. The proliferation of rectifier loads deteriorates the quality of voltage and current waveforms. Further, harmonic currents can lead to equipment overheating, malfunction of solid-state equipment, and interference with communication systems. IEEE 519 and IEC EN 61000-3 standards specify regulations governing harmonic compliance. The passive filter has been a viable approach because of low cost and high efficiency. However, the performance of the passive scheme has a limitation since the addition of the passive filter interfaces with the system impedance and causes resonance with other networks. Numerous active solutions which are becoming a more effective means to meet the harmonic standards by overcoming the drawback of the passive filter have been proposed. Active power filters (APFs) employing a pulse width-modulation (PWM) voltage-source inverter seem to be the most preferred scheme for canceling load harmonics. However, the general voltage-source inverter topology employs a relatively large dc-link capacitor to serve as a constant dc voltage source. Therefore, this scheme suffers from a bulky electrolytic capacitor, higher switching losses, and its associated dc-link voltage control issues due to reduced damping. In this paper, a three-phase active harmonic rectifier (AHR) scheme based on space-vector PWM (SVPWM) is proposed. The AHR module together with parallel-connected switch-mode rectifiers [Fig.1.1] is controlled to achieve clean input power characteristics. The AHR is compared with the APF based on
the analysis of VA power rating. The control system is designed on the synchronous reference frame where a low-pass filter to cancel harmonics offers better performance than the stationary reference frame. The converter fulfills harmonic cancellation as well as powering active power to its own load by PWM rectification. Therefore, the converter carries a fundamental current for active power and harmonics for the nonlinear loads.

Fig 1.1: Conventional Telecom rectifier power system (a) Telecom distributed rectifiers (b) Basic telecom rectifier topology
1.2. ADVANTAGES OF THE PROPOSED CONVERTER:

a) Reduced dc-link capacitor banks;

b) VA rating of the AHR is lower than that of the APF with rectifier current THD greater than 35%;

c) Better current control response;

d) Stable control system due to damping provided by the load;

e) No additional boost stage;

f) Efficient use of PWM rectifier.
Chapter 2

2. Power Quality

Today, the situation on low-voltage AC systems has become a serious concern. The quality of electrical power in commercial and industrial installations is undeniably decreasing. In addition to external disturbances, such as outages, sags and spikes due to switching and atmospheric phenomena, there are inherent internal causes specific to each site and resulting from the combined use of linear and non-linear loads.

Untimely tripping of protection devices, harmonic overloads, high levels of voltage and current distortion, temperature rise in conductors and generators all contribute to reducing the quality and the reliability of a low-voltage AC system. The current drawn from the AC mains has harmonic components, which causes to poor power factor, low efficiency, voltage and current distortion, interference in some instruments and communication equipment by the EMI, over heated transformers and electromagnetic fields and increased losses in transmission and distribution systems.

The above disturbances are well understood and directly related to the proliferation of loads consuming non-sinusoidal current, referred to as "non-linear loads”. This type of load is used for the conversion, variation and regulation of electrical power in commercial, industrial and residential installations.

Harmonic contamination has become a major concern for power system specialists due to its effects on sensitive loads and on the power distribution system. Therefore the compensation for harmonic and reactive current is important owing to the wide use of power electronic equipments. A classical solution is suitable power conditioning methodology such as passive filtering and active power filtering to suppress harmonics in power systems. Passive LC filters have been employed to eliminate line current harmonics and to improve the power factor. However, the harmonic problems still persists because of its inability to compensate random frequency variations in currents, tuning problems and parallel resonance.

Hence a very interesting solution is shunt active power filter, which is connected in parallel with the non – linear loads. The active power filter concept uses power electronics
to produce harmonic components, which cancel the harmonic components from the non-linear loads. Recently parallel connected-type active power filters have been developed for useful method of harmonic current compensation. In this work the proposed sunt active power filter has been modified and utilized for modern telecommunication rectifier power supply distribution.

2.1. Current detection methods

These active harmonic power filters are normally classified into two types on the basis of current detection methods.

1) Load current detection
2) Supply current detection

The former, which is popular than the latter, suppresses the source current harmonics indirectly with detecting the load current harmonics. The latter detects the source current and suppresses the source current harmonics directly.

Load current detection and supply current detection are suitable for shunt active power filters installed in the vicinity of one or more harmonic-producing loads by individual high-power consumers. This project will focus on the design, fabrication and the control methodology for a shunt active power filter used for telecommunication application named as a active harmonic rectifier (AHR). This method has the advantages of using only limited number of sensors, a simple control circuit and low implementation cost. A prototype is also developed to demonstrate the performance of this method. The test results show that the proposed active power filter has the expected performance. The active power filter is able to compensate the displacement of the input current in relation to the AC mains voltage and the harmonics components of single & multiple non-linear loads, through the sensing of the load current, which is the current controlled VSI PWM control technique. Active harmonic conditioners are proving to be viable option for controlling harmonic distortion levels in many applications.
2.2. Harmonic Fundamentals

- “A component frequency of a harmonic motion of an electromagnetic wave that is an integral multiple of the fundamental frequency”
- In other words, harmonics are currents or voltages with frequencies that are multiples of the fundamental frequency

![Diagram of Total current with harmonics](image)

2.3. HARMONIC DISTORTION:

It is well known harmonics are sinusoidal voltages or currents having frequencies that designed to operate usually 50 Hz or 60 Hz. Harmonics produce distortion in the waveform of the fundamental voltage or current. Harmonics distortion exists due to the nonlinear characteristics of the devices and loads on the power system. These devices are modeled as current sources that inject harmonic currents into the power system. Voltage distortion results as these currents cause non-linear voltages across the system impedance. Harmonic distortion is of growing concern for many customers and for the overall power
system due to increasing application of power electronics equipment.

2.4. IEEE 519 STANDARDS AND SOLUTIONS

2.4.1. IEEE 519 Standards

The most often quoted harmonics standard is IEEE 519, "Recommended Practices and Requirements for Harmonic Control in Electric Power Systems." IEEE 519 attempts to establish reasonable harmonic goals for electrical systems that contain nonlinear loads. The objective is to propose steady-state harmonic limits that are considered reasonable by both electric utilities and their customers. The underlying philosophy is that

- Customers should limit harmonic currents,
- Electric utilities should limit harmonic voltages,
- Both parties share the responsibility for holding harmonic levels in check.

IEEE 519 applies to all voltage levels, including 120V single-phase residential service. While it does not specifically state the highest-order harmonic to limit, the generally accepted range of application is through the 50th harmonic. Direct current, which is not a harmonic, is also addressed and is prohibited. Since no differentiation is made between single-phase and three phase systems, the recommended limits apply to both.

It is important to remember that IEEE 519 is a recommended practice and not an actual standard or legal document. Rather, it is intended to provide a reasonable framework within which engineers can address and control harmonic problems. It has been adopted by many electric utilities and by several state public utility commissions.

2.4.2. Definitions and terms

THD: Total Harmonic Distortion (or Distortion Factor) of voltage or current is the ratio of the RMS value of harmonics above fundamental, divided by the RMS value of the fundamental.

I_{sc}: Maximum short circuit current at the PCC.

I_L: Maximum demand load current (fundamental frequency component) at the PCC, calculated as the average current of the maximum demands for each of the proceeding twelve months. For new customers, this value must be estimated.

PCC: Point of Common Coupling is a point of metering, or any point as long as both the
utility and the customer can either access the point for direct measurements of the harmonic indices meaningful to both, or estimate the harmonic indices at the point of interference through mutually agreeable methods. Within an industrial load, the point of common coupling is the point between the nonlinear load and other loads.

**Utility Limits**

Electric utilities are responsible for maintaining voltage harmonics and *THVD*. The limits are divided into two categories: voltages 69KV and below, and voltages above 69KV. For electric utility distribution systems (i.e., corresponding to 69KV and below), are given in table 1.

**Customer limits**

Customers are responsible for maintaining current harmonics and *THID*. Again, the limits are divided into two categories: voltages 69KV and below, and voltages above 69KV. For 69KV and below, the limits are given in table 2.

There is some flexibility in determining the PCC, but in most instances, it is at the meter. An electric utility might also interpret the PCC to be on the high-voltage side of the service transformer, which would have the effect of allowing a customer to inject higher harmonic currents.

All power generation equipment is limited to these values of *THID*, regardless of the actual. Even ordered harmonics are limited to 25% of the odd harmonic limits given in the tables. Loads that produce direct current offset, e.g. half-wave converters.

### Table 1.2.1

<table>
<thead>
<tr>
<th>Bus voltage at PCC $(V_n)$</th>
<th>Individual Harmonic Voltage Distortion %</th>
<th>Total Voltage Distortion–THVD %</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_n \leq 69$ KV</td>
<td>3.0</td>
<td>5.0</td>
</tr>
<tr>
<td>$69$KV &lt; $V_n \leq 161$KV</td>
<td>1.5</td>
<td>2.5</td>
</tr>
<tr>
<td>$V_n &gt; 161$ KV</td>
<td>1</td>
<td>1.5</td>
</tr>
</tbody>
</table>
For PCC Voltages 69KV and Below Maximum $THID$ in % of $I_L$ for Odd harmonics $K$,

Table 2.2

<table>
<thead>
<tr>
<th>$I_{sc} / I_L$</th>
<th>$k&lt;11$</th>
<th>$11&lt;k&lt;17$</th>
<th>$17&lt;k&lt;23$</th>
<th>$23&lt;k&lt;35$</th>
<th>$&gt;35 k$</th>
<th>THID%</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;20</td>
<td>4.0</td>
<td>2.0</td>
<td>1.5</td>
<td>0.6</td>
<td>0.3</td>
<td>5.0</td>
</tr>
<tr>
<td>20 - 50</td>
<td>7.0</td>
<td>3.5</td>
<td>2.5</td>
<td>1.0</td>
<td>0.5</td>
<td>8.0</td>
</tr>
<tr>
<td>50 - 100</td>
<td>10.0</td>
<td>4.5</td>
<td>4.0</td>
<td>1.5</td>
<td>0.7</td>
<td>12.0</td>
</tr>
<tr>
<td>100 - 1000</td>
<td>12.0</td>
<td>5.5</td>
<td>5.0</td>
<td>2.0</td>
<td>1.0</td>
<td>15.0</td>
</tr>
<tr>
<td>&gt;1000</td>
<td>15.0</td>
<td>7.0</td>
<td>6.0</td>
<td>2.5</td>
<td>1.4</td>
<td>20.0</td>
</tr>
</tbody>
</table>

2.4.3. Solutions

Solutions techniques fall into two broad categories- preventive and remedial.

2.4.3.1 Preventive Measures

Preventive measures focus on minimizing harmonic currents that are injected into
power systems. Preventive measures include,

**a. Strict Adherence to IEEE 519.**

**b. Phase cancellation**

The use of twelve pulse converters instead of six pulse converters should be encouraged. Most utility harmonic problems are associated with the $5^{th}$ and $7^{th}$ harmonic currents, and if they are eliminated through phase cancellation, harmonic problem relay develop. In situations where there are multiple six pulse converters, serving half of them through delta-delta or wye-wye transformers and other half through wye-wye or delta-delta transformers, achieve net twelve pulse operation.

**c. Encouragement of low distorting loads**

Because of IEEE 519, increasing attention is being given to the THD of distorting loads. A customer often has a distortion choice in loads. For example, twelve pulse ASD’s and low-distortion fluorescent lamp ballasts can be purchased.

### 2.4.3.1. Remedial Measures

**a. Circuit detuning**

By using only field measurements such as capacitor current waveforms and search coli readings, it is possible to identify the capacitor banks that are most affected by resonance.

**b. Passive filters**

These are widely used to control harmonics, especially the $5^{th}$ and $7^{th}$ harmonics. Most filters consist of series L and C components that provide a single tuned notch with a low impedance ground path. At 50 / 60 Hz, these filters are for all practical purposes, capacitors. Thus passive filters provide both power factor correction and voltage distortion control. Usually higher the harmonic, the fewer KVARs needed for filter. For multiple filter installations, a good practice is to stair step the KVARs as follows.

If Q KVARs are used for the $5^{th}$ harmonic, then Q / 2 should be used for the $7^{th}$ harmonic, Q / 4 for the $11^{th}$ harmonic and Q / 8 for the $13^{th}$ and so on. For best performance, filter should be at least 300 KVAR.

Their effectiveness diminishes over time as their capacitor age, losing Capacitance and raising their notching frequency. They attract harmonic currents from all sources in the
network – new, known, and unknown, so that they become overloaded.

c. Active power filters

This is a new promising technology, but there are as yet few distribution feeder installations. Active filters are power electronic converters that inject equal – but – opposite distortion to yield more sinusoidal voltage waveforms thought a network. Active filters have the advantages of:

* Time domain operation so that they automatically “tune” to the harmonics.
* Current limiting capability to prevent overload by new or unknown sources of harmonics on the network.
* Multi – point voltage monitoring so that they can simultaneously minimize distortion at local and remote buses.

The objective of “Who is responsible for installing active filters”, classifies them into the following two groups:

1. Active filters installed by individual consumers on their own premises near one or more identified harmonic producing loads.
2. Active filters installed by Electric Power Utilities in Substations and / or on distribution Feeders.

Chapter 3

3. TELECOM POWER SYSTEM

Modern telecommunication systems require a higher dc power. An example system requirement consists of 48 Vdc and 800 A (38.4 kW). All of the equipment runs on dc voltage generated by ac-fed redundant rectifiers of which the purpose is to supply power to the equipment. Fig. 3.1(a) shows a distributed rectifier system where a three-phase utility power is transferred into 48 Vdc. The telecom rectifiers consist of a rectifier stage, a dc-to-dc converter, and a battery backup system. The major portion of the load is the logic circuitry in board-mounted power (BMP) converter units used to convert 48 V to 5 V and 12 V. The purpose of the dc–dc converter is to transfer high dc-link voltage to lower voltage 48 V and provide isolation. Each paralleled dc–dc converter module requires a current-
sharing mechanism to ensure even current distribution. A battery backup system on the 48-V dc bus is required to support the critical loads in case of utility failure. The basic topology of the telecom rectifier is shown in Fig. 1(b). The boost stage is used only to regulate dc-link voltage for a wide input voltage range. Since the power supply employs diode rectifiers because of economic reasons, the high-power rectifiers result in more serious problems related to harmonic currents. Such a typical rectifier may have more than 30% THD of input current. Fig. 3.1. Shows an example of a telecommunication power system (An AHR [Fig. 3(a)] or APF [Fig. 2(b)] is embedded in a rectifier slot and is rack mountable so that the THD in the utility current can be improved by eliminating harmonic contents. The AHR with harmonic filtering function supplies active power and harmonic currents while the APF generates load harmonics and optional reactive power.
Fig. 3.1. Example telecom power system as a plug-in rack-mountable module (a) Rectifier system with AHR (P = 38.4 kW). (b) Rectifier system with APF

3.1. PROPOSED TOPOLOGY:

In this project, a three-phase active harmonic rectifier (AHR) scheme based on time domain extraction techniques is proposed. The AHR module together with parallel-connected switch-mode rectifiers is controlled to achieve clean input power characteristics. The AHR is compared with the APF based on the analysis of VA power rating. The converter fulfills harmonic cancellation as well as powering active power to its own load by PWM rectification. Therefore, the converter carries a fundamental current for active power and harmonics for the nonlinear loads.

3.2. PROPOSED AHR SCHEME FUNCTIONAL BLOCK DIAGRAM

Fig. 3.2 shows the basic harmonic cancellation techniques using AHR. The proposed AHR scheme (Fig. 3.3) consists of rectifier nonlinear loads, three-leg PWM rectifier, paralleled dc–dc converters, and battery backup system. Since rectifier load produces harmonic currents such as the 5th, 7th, etc., a PWM rectifier with active harmonic filtering capability,
called the AHR, compensates for load harmonics as well as supplying active power to its own load. The AHR carries a fundamental current for active power and harmonics for the nonlinear loads to make the input current sinusoidal. **Fig.3.4** shows the current waveforms for the rectifier input, AHR, and utility currents. The reactive power of the load also can be optionally to control the active harmonic rectifier; bidirectional power flows are required for 5th and 7th harmonic currents. The input source current is defined as:

\[
  i_s = N i_L - i_F
\]

---------------3.1

Where \(i_s\), \(N i_L\) and \(i_F\) denote utility, load, and APF currents respectively. The rms harmonic currents of the AHR and APF are relatively given as

\[
  i_{F,har} = (N - 1) \cdot i_{L,har} \\
  i_{F,har} = N \cdot i_{L,har}
\]

---------------3.2

The harmonic current of the AHR is \((N-1/N)\) times the APF harmonic currents. The VA ratings of the proposed AHR with and without reactive power compensation are, respectively, where the subscript denotes a nonlinear load. In the case

For Active Harmonic Rectifier

\[
  VA_{AHR} = \sqrt{\frac{\alpha \cos^2 \phi + (N-1)^2 THD_{NL}^2}{1 + THD_{NL}^2}} \cdot VA_{NL}, \text{ (without)}
\]

---------------3.3

\[
  VA_{AHR} = \sqrt{\frac{(N-1)^2 (\sin^2 \phi + THD_{NL}^2) + \cos^2 \phi}{1 + THD_{NL}^2}} \cdot VA_{NL}, \text{ (with)}
\]

---------------3.4

For Active Power Filter
Fig. 3.2. Functional Block Diagram of Proposed Telecommunication Power distribution network

\[ V_{A_{	ext{ATF}}} = \sqrt{\frac{THD_{N}^{N} + \frac{8\sin^{2}\theta}{1+THD_{N}^{N}}} \cdot N \cdot V_{A_{NL}}} \]
Fig: 3.3. Active harmonic filtering techniques in telecom distributed system AHR (b) APF

Figure. 3.4. Current waveforms for the proposed AHR scheme

Chapter 4

4. Reference Signal Estimation Techniques
As shown in Figure the reference signal to be processed by the controller is the key component that ensures the correct operation of APF. The reference signal estimation is initiated through the detection of essential voltage/current signals together accurate system variables information. The voltage variables to be sensed are AC source voltage, DC-bus
voltage of the APF, and voltage across interfacing transformer. Typical current variables are load current, AC source current, compensation current and DC-link current of the APF. Based on these system variables feedbacks, reference signals estimation in terms of voltage/current levels are estimated in frequency-domain or time-domain. Figure 2.14 illustrates the considered reference signal estimation techniques. These techniques cannot be considered to belong to the control loop since they perform an independent task by providing the controller with the required reference for further processing.

Figure: 4.1.Subdivision of reference signal estimation techniques

4.1. Frequency Domain Approaches

Reference signal estimation in frequency-domain is suitable for both single and three phase systems. It is mainly derived from the principle of Fourier analysis as follows.

4.2. Fourier Transform Techniques
In principle, Fourier Transform (either conventional or Fast Fourier Transform (FFT)) is applied to the captured voltage/current signal. The harmonic components of the captured voltage/current signal are first separated by eliminating the fundamental component. Inverse Fourier Transform is then applied to estimate the compensation reference signal in time domain. The main drawback of this technique is the accompanying time delay in system variables sampling and computation of Fourier coefficients. This makes it impractical for real-time application with dynamically varying loads. Therefore, this technique is only suitable for slowly varying load conditions.

4.3. Time Domain Approaches

Time-domain approaches are based on instantaneous estimation of reference signal in the form of either voltage or current signal from distorted and harmonic polluted voltage and current signals. These approaches are applicable for both single-phase and three-phase systems except for the synchronous-detection theorem and synchronous-reference-frame theorem which can only be adopted for three-phase systems.

4.4. Instantaneous Reactive-Power Theorem

The instantaneous reactive-power (p-q) theorem is proposed by Akagi et al [57]. This theorem is based on αβ0 transformation which transforms three-phase voltages and currents into the αβ0 stationary reference frame. From this transformed quantities, the instantaneous active and reactive power of the nonlinear load is calculated, which consists of a DC component and an AC component. The AC component is extracted using HPF and taking inverse transformation to obtain the compensation reference signals in terms of either currents or voltages. This theorem is suitable only for a three-phase system and its operation takes place under the assumption that the three-phase system voltage Waveforms are symmetrical and purely sinusoidal. If this technique is applied to contaminated supplies, the resulting performance is proven to be poor. In order to make the p-q theorem applicable for
single-phase system, some modifications in the original p-q theorem were proposed and implemented by Dobrucky et al.

4.5. Control Techniques for Active Harmonic Rectifier

The aim of APF control is to generate appropriate gating signals for the switching transistors based on the estimated compensation reference signals. The performance of an APF is affected significantly by the selection of control techniques. Therefore, the choice and implementation of the control technique is very important for the achievement of a satisfactory APF performance. A variety of control techniques, such as linear control, digital deadbeat control, hysteresis control etc., have been implemented for the APF applications.

4.6. Linear Control Technique

Linear control of an APF is accomplished by using a negative-feedback system as shown in Figure. In this control scheme, the compensation current \( i_f \) or voltage \( v_f \) signal is compared with its estimated rated reference signal \( i_{f_{\text{ref}}} \) or \( v_{f_{\text{ref}}} \) through the compensated error amplifier to produce the control signal. The resulting control signal is then compared with a saw tooth signal through a pulse width modulation (PWM) controller to generate the appropriate gating signals for the switching transistors. The frequency of the repetitive saw tooth signal establishes the switching frequency. This frequency is kept constant in linear control technique. As shown in Figure, the gating signal is set high when the control signal has a higher numerical value than the saw tooth signal and vice versa. With analogue PWM circuit, the response is fast and its implementation is simple. Nevertheless, due to inherent problem of analogue circuitry, the linear control technique has an unsatisfactory harmonic compensation performance. This is mainly due to the limitation of the achievable bandwidth of the compensated error amplifier.
The size determination of the DC-bus capacitor is based on the energy balance principle. Using this concept, the following equations can be derived:

The size of DC-bus capacitor is determined by:

\[
C_f \geq \frac{\sqrt{2V_i \cdot \Delta I_L \cdot T/2}}{2 \cdot (\Delta V_{cf})^2 - (V_{cf,eq})^2}
\]

--------4.1

The minimum interfacing inductor \((L_{fmin})\) can be calculated based on as:

\[
L_{f,ma} = \frac{V_{cf}}{2 \cdot (\Delta I_{sw,p-p}) \cdot f_{sw,ma}}
\]

--------4.2

Where \(f_{sw,ma}\) is the maximum frequency of switching ripple and \(\Delta I_{sw,p-p}\) is the peak-to-peak switching ripple of compensation current
Control of the proposed AHR

Based on the fundamental concept, the non linear load current $I_L$ is sensed by a current transducer. The sensed $I_L$ is passed through a band pass filter to filter out fundamental components of the $I_L$. Then the extracted fundamental component is subtracted from the total harmonic load current. Also in additional, a 50Hz twin T notch filter is used to extract the power line hum. Now, the output of the extraction circuit is a signal containing purely the harmonic component of load current. In the extraction circuit, realization of biquad filtering method is used as the extraction topology. This method uses a Tow-Thomas biquad band-pass filter (shown in Figure 4.3 and a difference amplifier circuit. The band pass filter is designed to be 50 Hz with unity gain and quality factor of 5. This harmonic signal is used to control the firing topology of the PWM rectifier. It is a single phase representation and it can be extended for three phase with same logic. Transfer function obtained from test circuit is given by,

$$\frac{V_o}{V_i} = \frac{62.5S}{S^2 + 62.5S + 97656}$$
Chapter 5

Simulation results

![Diagram of rectifier fed nonlinear load model](image)

Fig. 5.1. Non Linear load model
Fig 5.2. Simulation results of load current, source current and source voltage.

Fig. 5.3. Simulation circuit of Telecommunication power supply system.
Fig. 5.4. Simulation results of load current, source current and source voltage
Fig: 5.5. Proposed Single phase AHR used for telecommunication rectifier system
Fig 5.6. Simulation results of load current, source current and source voltage without AHR compensation
Fig 5.7. Simulation results of load current, source current and source voltage with AHR compensation

Fig. 5.8. Battery voltage
**SIMULATION DESIGN VALUES:**

An AHR design is based on the telecommunication rectifier system shown in Fig. The total rectifier VA rating is 50kVA.

The AHR design specifications are as follows:

- a) Input voltage: 220 V
- b) Input current: 200A
- c) DC bus voltage: 400V
- d) Input inductor: 1mH
- e) Filter current: 50A
- f) Load current: 200A
- g) Output capacitor: 1000uF
- h) Switching frequency: 20 kHz.
- i) Filter inductance: 1mH
- j) DC bus capacitor: 470uF
- k) Switching Devices: MOSFET IRFP460, 18 A, 500 volts

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**Chapter 6**

**6. HARDWARE IMPLEMENTATION OF PROPOSED ACTIVE HARMONIC RECTIFIER**

The proposed active harmonic rectifier system is implemented on a Prototype hardware module. A proportional–integral (PI) current controller regulates harmonic current and SPWM technique is employed for the voltage-source inverter. **Fig.** shows the control performance of the proposed scheme from experimental results without reactive power compensation. The AHR compensates load harmonics and supplies active power. The AHR current contains a fundamental component and load harmonics while the APF generates only load harmonic currents.
6.1. Control Techniques for Active Harmonic Rectifier

The aim of AHR control is to generate appropriate gating signals for the switching transistors based on the estimated compensation reference signals. The performance of an AHR is affected significantly by the selection of control techniques. Therefore, the choice and implementation of the control technique is very important for the achievement of a satisfactory AHR performance. A variety of control techniques, such as linear control, digital deadbeat control, hysteresis control etc., have been implemented for the AHR applications. In this project linear control techniques using simple time domain harmonic extraction techniques are proposed.
6.2. Nonlinear Load

The nonlinear load used in the experimental prototype is a single-phase full bridge diode rectifier feeding Battery supplying load. The DC smoothing capacitor ($C_{dc}$) consists of a 1000 μF, 250V DC electrolytic capacitor.

6.3. HARDWARE PROTOTYPE DESIGN VALUES

An AHR design is based on the telecommunication rectifier system shown in Fig. The total rectifier VA rating is 1kVA. The AHR design specifications are as follows:

- Input voltage: 220/0-24 VOLTS V;
- Input current: 3A;
- Dc bus voltage: 40V
- Input load inductor: 1mH
- Filter current: 18A max
- Load current: 6A
- Output capacitor: 1000uF
- Switching frequency: 20 kHz.
- Filter inductance: 10mH
- DC bus capacitor: 470Uf

Switching Devices used

- Active Harmonic Rectifier
  - MOSFET IRFP460, 18 A, 500 volts
- DC-DC converter
  - IRP 450, 500 volt, 14 A

6.4. Harmonic extraction circuit using Band pass Filter Approach
Based on fundamental concept, the non-linear load current $I_L$ is sensed by a current transducer. The sensed $I_L$ is passed through a Band Pass filter to filter out fundamental components of the $I_L$. Then the extracted fundamental component is subtracted from the total harmonic load current. Now, the output of the extraction circuit is a signal containing purely the harmonic component of load current. The block diagram representation with associated circuit diagram is shown in Fig.2

**6.4.1. Bands reject filter (Band pas + Difference Amplifier) or 50Hz Twin T Notch Filter response**

The notch filter given in Fig. which is useful for the rejection of a single frequency such as 50 Hz power line frequency hum of is to extract the harmonic content of the non-linear load current. Notch-out frequency is given by

$W_0 = 1/RC$ which is tuned as the 50 Hz line frequency

Bandwidth $BW = f_h - f_l = 4(1-K) F_0$ where $K = R2/ (R1+R2)$,

Quality factor $Q = F_0/BW$

In this notch filter, an adjustable positive feedback voltage is added through a voltage follower to the common terminal of the filter network in order to control the bandwidth of the filter. Positive feedback, in contrast to negative, decreases the bandwidth and thus increases the Quality factor of the circuits. Keeping $R4$ constant, $Q$ is entirely adjusted by $R3$, which determines the percentage of the feedback voltage.

The high frequency attenuation is in fact characterized by the limited bandwidth of the common 741 operational amplifiers. Using a wide-bandwidth operational amplifier such as CA3140E can extend the operating bandwidth.
The purpose of introducing the triangular waveform is to stabilize the converter switching frequency by forcing it to be constant and equal to the frequency of the harmonic reference signal, which are multiples of fundamental signals. Since the current reference signal is always kept within the negative and positive peaks of the triangular waveform generation of triangular carrier wave is given in Fig.4.

The peak amplitude of triangular waveform is given by

$$ V_o (pp) = 2.R_2/R_3 . V_{cc} $$

The output frequency of oscillation is given by

$$ F_0 = R_3/4R_1C_1R_2 $$
For varying the values of resistance R1 with fixed values of R3a and R2 the output frequency $F_o$ can be varied.
6.6. **PWM control strategy**

In a PWM, the two signals required are the Reference signal and Carrier signal. The harmonic signal from the extraction acts as the reference signal for this PWM Generator and the carrier signal used is the Triangular wave. The control of the output current of this shunt active power filter is based on full-bridge VSI. The VSI method used in this work is the sinusoidal PWM. Inverters that operate under this scheme are also known as “PWM Power Amplifier”. The usual practice is that the frequency of the carrier wave is at least three times that of the harmonic frequency. The switching frequency of the SPWM inverter is the average rate at which the circuit develops output pulses and is determined by the frequency of the triangular waveform. In this active filter application, the higher the relative switching frequency, the more fidelity to the reference signal is obtained. However, there are two factors that imposes limit to the switching frequency of SPWM. They are switching frequency capability of the IGBT, and the increase in switching losses, which is proportional to high switching frequency. The switching losses will reduce the circuit efficiency. Hence, there must be a compromise between fidelity and efficiency.

The output of the VSI is connected to a LC low-pass interfacing filter (Switching Ripple Filters) via synchronous link reactor to provide a sufficient attenuation of the high switching ripples caused by the VSI. Hence the adopted solution to this output filtering is the combined use of an ordinary second order LC low pass filter with or without damping branch consists of RC circuit.
PWM Control circuit specification

Triangular carrier switching frequency: 10 - 20 KHz

Triangular peak amplitude: 10.0 V

Modulation index \( M : V_{\text{TRI}} / V_{\text{REF}} \)

\( V_{\text{REF}} \) is proportional to harmonic current reference signal. Hence modulation index is automatically tuned with Harmonic current reference signal obtained from the current sensor.

6.7. Power MOSFET / IGBT’S Gate Driver Circuit:

For the full bridge converter in the APF, the gate driving signals for those two upper switches S1 and S2 should be floating. Father more, the conventional limited bandwidth pulse transformer is not suitable to be applied since the switching frequency is variable for the PWM hysterics controller. To meet all the requirements, a high voltage high side driver IC IR2110 is suitable manufactured by the National Semiconductor, which is driving stage floating up to 600V. Its recommended operating frequency ranges from DC to 250 KHz. Typical connection of driver circuit is given in Fig.5
6.8. Power circuit design criteria

6.8.1. Filter inductor:

A series inductor at VSI Bridge working as an APF is normally used as the buffer between supply terminal voltage and PWM voltage generated by the APF’s. The value of this inductor is very crucial in the performance of the AF’s. If small value of inductor is selected, then large switching Ripples are injected into the supply currents, and a large value of Inductance does not allow proper tracking of the compensating currents close to the desired values. An optimum selection of Inductance is essential to obtain satisfactory performance of the APF. The simple design formula used for selection of filter inductor is given by

The minimum interfacing inductor \((L_{fmin})\) can be calculated based on as:

\[
L_{f_{min}} = \frac{V_f}{2 \cdot (\Delta f_{P,V} - \Delta f_{P,V_{in}}) \cdot f_{min}}
\]

-------------6.1
Filter inductor $L_F$ stems from a fact, which is used to produce compensating harmonic current, which is in phase opposition to harmonic current.

**6.8.2. Switching Ripple Filters**

The output of the VSI is connected to a LC low pass-interfacing filter to provide a sufficient attenuation of the high switching ripples caused by the VSI. Hence the adopted solution to this output filtering problem is the combined use of an ordinary second order LC low pass filter with a damping branch consists of RC. The different configuration of output low pass filter in order to attenuate switching ripples is shown in figure.

![Configuration of switching ripple filters](image)

**Fig: Configuration of switching ripple filters**

Generally passive LC filter is used at the terminal of supply system, which compensates for switching harmonics and improves the THD of the supply voltage and current. The design of the switching ripple filter is also important, because source impedance can cause an interaction with its components. Second order LC Low pass filter is sufficient for eliminating switching ripples of the inverter. Second order LC or LCL filter which is including filter inductor is given by

**6.8.3. Filter Capacitor**

The dc bus Capacitor value $C_{dc}$ of the APF’s is another important
parameter. With a small value of Capacitance, large ripples in the steady state and wide fluctuations in the dc bus voltage under transient conditions are observed. A higher value of Capacitance Reduces ripples and fluctuations in the dc bus voltage but increase the cost and size of the system.

The size of DC-bus capacitor is determined by:

\[ C_f \geq \frac{\sqrt{2}V_c \cdot \Delta I_{L} \cdot T/2}{(\Delta V_{Cf})^2 - (V_{Cf,ref})^2} \]

Where \( f_{sw,ma} \) is the maximum frequency of switching ripple and \( \Delta I_{sw,p-p} \), is the peak-to-peak switching ripple of compensation current.

Chapter 7

7. DC-DC CONVERTER - HARDWARE DESCRIPTION

The Analysis and Design of a high conversion ratio DC-DC converter used for Telecommunication supply systems is implemented in hardware. The pulses for the converter switches are obtained from IC-TL084CN. The frequency of operation is 25 kHz. TL084CN adjusts the duty ratio of the gate pulses for the variation in input or load to maintain the load voltage constant.

The hardware consists of four main parts

1. Power supply unit
2. PWM pulse generator unit
3. Driver circuit unit

4. Power Elementary circuit

**7.1. DESIGN OF POWER SUPPLY UNIT**

The following devices are used to design the power supply unit

1. Step down transformer (230/15v, 1A)

2. Diodes (DIN4007) - 4 NOS

3. Filter capacitor $C_1 = 2200 \text{Micro Farad}$
   $C_2 = C_3 = 0.1 \text{ Micro Farad}$
   $C_4 = 470 \text{ Micro Farad}$

4. Voltage regulator 7812 -1C.

The power supply diagram is given below,
7.2. DESIGN OF PWM GENERATOR UNIT

The PWM generator which is used in the hardware is shown in the below Fig. 6.2. It uses TL084CN –IC to generate PWM pulse. This IC consists of four operational amplifiers. U1c is used to generate a 6 Volt reference current which is used as a virtual ground for the oscillator, this is necessary to allow the oscillator to run off of a single supply instead of a +/- voltage dual supply. U1d is the triangular wave generator.

U1a is the square wave generator. The triangular wave and the voltage divider voltage (5V) are given to the comparator. U1b is the comparator which compares the triangular wave with fixed dc voltage.

U1b is wired in a comparator configuration and is the part of the circuit that generates the variable pulse width. By varying the pin 6 voltage, the on/off points are moved up and down the triangle wave, producing a variable pulse width waveform. This waveform is obtained in PIN no.7. The resistances R2, R1, R3, and C1 determines the frequency of PWM

**FREQUENCY OF PWM:**

\[
\text{frequency} = \frac{R2}{4 R1 R3 C1}
\]

\[
= \frac{22 \times 10^3}{4 \times 2.2 \times 10^3 \times 10^3 \times 0.01 \times 10^{-6}}
\]
= 25 K HZ

**VOLTAGE OF PWM:**

= 2*5 = 10V

**VOLTAGE OF TRIANGULAR WAVE**

\[ V_c = \frac{R_3 \times V_{cc}}{R_2} \]

= \frac{10 \times 10^3 \times 12}{22 \times 10^3}

= 5v

The following devices are used to design the PWM generator.

**TL084CN –IC FOR PWM GENERATOR**, R1- 2.2K, R2- 22K, R3-10K, C1- 0.01UF, R7-100K, R8-100K, R5-10K, R4-3.3K, R5-33K
7.3. DESIGN OF DRIVER CIRCUIT:

The **IR2110** is high voltage, high speed power MOSFET driver with independent high and low side referenced output channels. The design of the
driver circuit is given below 6.3.

**IR2110- DRIVER IC**, R9, R10-22 OHM, C3, C5- 4.7UF, C2,C4-0.01UF,C8 -10UF,D1 –IN4500

![Typical Connections to IR2110 Driver IC](image)

**Fig.7.2 Typical Connections to IR2110 Driver IC**
Chapter 8

8. Hardware Components Description

8.1. CA3140A High performance industrial operational amplifier

4.5MHz, BiMOS Operational Amplifier with MOSFET Input/Bipolar output. The CA3140A and CA3140 are integrated circuit operational amplifiers that combine the advantages of high voltage PMOS transistors with high voltage bipolar transistors on a single monolithic chip.

The CA3140A and CA3140 Bi MOS operational amplifiers feature gate protected MOSFET (PMOS) transistors in the input circuit to provide very high input impedance, very low input current and high-speed performance. The CA3140A and CA3140 operate at supply voltage from 4V to 36V (either
single or dual power supply). These operational amplifiers are internally phase compensated to achieve stable operation in unity gain follower operation, and additionally, have access terminal for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input /offset voltage null. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute for single supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load terminal short-circuiting to either supply rail or to ground. The CA3140A and CA3140 are intended for operation at supply voltages up to 36V (±18V).

Features

- MOSFET Input Stage
- Very High Input Impedance
- Very Low Input Current
- Wide Common Mode Input Voltage Range
- Swing 0.5V below Negative Supply Voltage Rail
- Output Swing Complements Input Common Mode Range
- Directly Replaces Industry Type 741 in Most Applications

Applications

- Ground-Referenced Single Supply Amplifiers in Automobile and Portable Instrumentation
- Sample and Hold Amplifiers
- Long Duration Timers/ Multivibrators
- Photocurrent Instrumentation
- Peak Detectors
- Active Filters
- Comparators
- Interface in 5V TTL Systems and Other Low Supply Voltage Systems
- All Standard Operational Amplifier Applications
- Function Generators
- Tone Controls
- Power Supplies
- Portable Instruments
- Intrusion Alarm Systems

**Pin details of CA 3140E**

Device specifications CA3140E

Absolute Maximum Ratings

DC Supply Voltage (Between V+ and V- Terminals) .......... 36V
Differential Mode Input Voltage ................................. 8V
DC Input Voltage ........................................... (V+ +8V) To (V- -0.5V)
Input Terminal Current ....................................... 1mA
Output Short Circuit Duration: Indefinite

Operating Conditions

Temperature Range: -55°C to 125°C
Temperature (Plastic Package): 150°C
Maximum Storage Temperature Range: -65°C to 150°C
Maximum Lead Temperature (Soldering 10s): 300°C

8.2. LF347/TLO84CN Quad Operational Amplifier (JFET)

Features

• Low input bias current
• High input impedance
• Wide gain bandwidth: 4 MHz
• High slew rate: 13 V/S

Description

The LF347 is a high-speed quad JFET input operational amplifier. This feature high input impedance, wide bandwidth, high slew rate, and low input offset voltage and bias current. LF347 may be used in circuits requiring high input impedance. High slew rate and wide bandwidth, low input bias current.

Absolute maximum rating

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>Vcc</td>
<td>±18</td>
<td>V</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>V( DIFF)</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>V1</td>
<td>±15</td>
<td>V</td>
</tr>
<tr>
<td>Output Short Circuit Duration</td>
<td></td>
<td>Continuous</td>
<td></td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>PD</td>
<td>570</td>
<td>mW</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>TCPR</td>
<td>6...+70</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>TSTG</td>
<td>-65...+150</td>
<td>°C</td>
</tr>
</tbody>
</table>

TL084CN op-amp IC:
8.3. DESIGN OF DRIVER CIRCUIT:

The IR2110 is a high voltage, high speed power MOSFET driver with independent high and low side referenced output channels. The design of the driver circuit is given below.

**Features**

- Floating channel designed for bootstrap operation
- Fully operational to +500V or +600V
- Tolerant to negative transient voltage
- DV/DT immune
- Gate drive supply range from 10 to 20V
- Under voltage lockout for both channels
- 3.3V logic compatible
- Separate logic supply range from 3.3V to 20V
- Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
• Cycle by cycle edge-triggered shutdown logic
• Matched propagation delay for both channels
• Outputs in phase with inputs

Description

The IR2110/IR2113 is high voltage, high-speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable rugged monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output driver’s feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration, which operates up to 500 or 600 volts.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages.
referred to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VB</td>
<td>High side floating supply voltage (\text{(IR2110)})</td>
<td>-0.3</td>
<td>525</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(\text{(IR2113)})</td>
<td>-0.3</td>
<td>625</td>
<td>V</td>
</tr>
<tr>
<td>VS</td>
<td>High side floating supply offset voltage</td>
<td>(\text{VB} - 25)</td>
<td>(\text{VB} + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>VTHO</td>
<td>High side floating output voltage</td>
<td>(\text{VS} - 0.3)</td>
<td>(\text{VB} + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>VCC</td>
<td>Low side fixed supply voltage</td>
<td>-0.3</td>
<td>25</td>
<td>V</td>
</tr>
<tr>
<td>VLO</td>
<td>Low side output voltage</td>
<td>-0.3</td>
<td>(\text{VCC} + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>VDD</td>
<td>Logic supply voltage</td>
<td>-0.3</td>
<td>(\text{VSS} + 25)</td>
<td>V</td>
</tr>
<tr>
<td>VSS</td>
<td>Logic supply offset voltage</td>
<td>(\text{VDD} - 25)</td>
<td>(\text{VCC} + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>VIN</td>
<td>Logic input voltage (\text{(HN, LN &amp; SD)})</td>
<td>(\text{VSS} - 0.3)</td>
<td>(\text{VDD} + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>dVs/dt</td>
<td>Allowable offset supply voltage transient (\text{(figure 2)})</td>
<td>—</td>
<td>50</td>
<td>V/\mu \text{s}</td>
</tr>
<tr>
<td>PD</td>
<td>Package power dissipation (\text{@ } T_A \leq +25^\circ \text{C}) (\text{(14 lead DIP)})</td>
<td>—</td>
<td>1.6</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>(\text{(16 lead SOIC)})</td>
<td>—</td>
<td>1.25</td>
<td>W</td>
</tr>
<tr>
<td>RTJUA</td>
<td>Thermal resistance, junction to ambient (\text{(14 lead DIP)})</td>
<td>—</td>
<td>75</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td>(\text{(16 lead SOIC)})</td>
<td>—</td>
<td>100</td>
<td>°C/W</td>
</tr>
<tr>
<td>TJ</td>
<td>Junction temperature</td>
<td>—</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>TS</td>
<td>Storage temperature</td>
<td>-55</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>TL</td>
<td>Lead temperature (\text{(soldering, 10 seconds)})</td>
<td>—</td>
<td>300</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Recommended Operating Conditions**

For proper operation the device should be used within the recommended conditions. The VS and VSS offset ratings are tested with all supplies biased at 15V differential.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VB</td>
<td>High side floating supply absolute voltage</td>
<td>(\text{VS} + 10)</td>
<td>(\text{VS} + 20)</td>
<td>V</td>
</tr>
<tr>
<td>VS</td>
<td>High side floating supply offset voltage (\text{(IR2110)})</td>
<td>(\text{Note 1})</td>
<td>500</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(\text{(IR2113)})</td>
<td>(\text{Note 1})</td>
<td>500</td>
<td>V</td>
</tr>
<tr>
<td>VTHO</td>
<td>High side floating output voltage</td>
<td>(\text{VS})</td>
<td>(\text{VB})</td>
<td>V</td>
</tr>
<tr>
<td>VCC</td>
<td>Low side fixed supply voltage</td>
<td>10</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>VLO</td>
<td>Low side output voltage</td>
<td>0</td>
<td>(\text{VCC})</td>
<td>V</td>
</tr>
<tr>
<td>VDD</td>
<td>Logic supply voltage</td>
<td>(\text{VSS} + 3)</td>
<td>(\text{VSS} + 20)</td>
<td>V</td>
</tr>
<tr>
<td>VSS</td>
<td>Logic supply offset voltage</td>
<td>(-5) (\text{(Note 2)})</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td>VIN</td>
<td>Logic input voltage (\text{(HN, LN &amp; SD)})</td>
<td>(\text{VSS})</td>
<td>(\text{VDD})</td>
<td>V</td>
</tr>
<tr>
<td>TA</td>
<td>Ambient temperature</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>
8.4. Typical Connections to IR2110 Driver IC:

Driver circuit

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Logic supply</td>
</tr>
<tr>
<td>HIN</td>
<td>Logic input for high side gate driver output (HC), in phase</td>
</tr>
<tr>
<td>SD</td>
<td>Logic input for shutdown</td>
</tr>
<tr>
<td>LIN</td>
<td>Logic input for low side gate driver output (LO), in phase</td>
</tr>
<tr>
<td>VSS</td>
<td>Logic ground</td>
</tr>
<tr>
<td>VB</td>
<td>High side floating supply</td>
</tr>
<tr>
<td>H0</td>
<td>High side gate drive output</td>
</tr>
<tr>
<td>V5</td>
<td>High side floating supply return</td>
</tr>
<tr>
<td>VCC</td>
<td>Low side supply</td>
</tr>
<tr>
<td>LO</td>
<td>Low side gate drive output</td>
</tr>
<tr>
<td>COM</td>
<td>Low side return</td>
</tr>
</tbody>
</table>
8.5. MOSFET IRFP450

SPECIFICATIONS

<table>
<thead>
<tr>
<th>TYPE</th>
<th>$V_{DSS}$</th>
<th>$R_{DS(on)}$</th>
<th>$I_D$</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRFP450</td>
<td>600 V</td>
<td>&lt; 0.4 Ω</td>
<td>14 A</td>
</tr>
</tbody>
</table>

- TYPICAL $R_{DS(on)} = 0.33$ Ω
- EXTREMELY HIGH $dv/dt$ CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

APPLICATIONS

- UNINTERRUPTIBLE POWER SUPPLY (UPS)
- HIGH CURRENT SWITCHING
- DC/DC CONVERTERS FOR TELECOM,
- INDUSTRIAL, AND LIGHTING Equipments

CONCLUSION

The design of AHR has been presented in this work. These types of harmonic filter allow the harmonics present in the utility system to be filtered out without jeopardizing the stability of the system and hence, providing a good quality of power supply to the customer side.
Design of Passive filter is based on fundamental frequency reactive power required for power factor correction and harmonic current compensation. It is good alternative for current harmonics compensation and displacement power factor correction. Another technical disadvantage of passive filters is related to the small design tolerances acceptable in the values of inductor and capacitor. And also individual harmonic current only compensated. In order to overcome these problems active filter is designed, which is based on the sinusoidal PWM VSI topology to compensate simultaneously all the order of harmonics.

However the main problem associated with active power filter is increased in ratings of devices causes more switching losses and increased cost of the system. Another approach of harmonics filtering is based on hybrid topology in which case the compensation performance of passive filter was improved with the active techniques. It was identified that the hybrid topology improves the compensation characteristics of passive filters, and allows the use of active power filters used in high power applications at a relatively low cost.

FUTURE WORK

The performance of AHR will be implemented by developing different methods of hardware circuitry. The performance of active Filter can be checked with investigation carried out in hardware. Their performance can be further improved by an improvement in the design of harmonic extraction circuit, PWM control circuit and the LP filter for interfacing the active filter and the utility system. Hardware is implemented with unbalanced system, it is possible to redistribute and equilibrate the mains phase currents, providing that the total amount of power coming from the mains same as the amount required for the load.